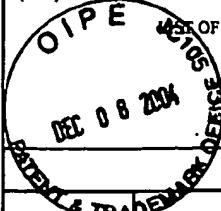


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			455610-2590.2		10/673,735		
LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)			APPLICANT				
			Martin MILLER et al.				
			FILING DATE		GROUP		
			September 29, 2003		2133		
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
PC	AA	4,633,465	12/30/86	Fitch et al.			
PC	AB	5,337,403	08/09/94	Klingman	V	V	
	AC						
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FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES
	AL						NO
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	AN						
	AO						
	AP						
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EXAMINER /Phung Chung/				DATE CONSIDERED 07/07/2006			
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				FILING DATE September 29, 2003	GROUP 2133		
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
PC	AA	5,654,987	08/05/97	Nakamura			
	AB	5,726,607	03/10/98	Brede et al			
	AC	5,825,825	10/20/98	Altmann et al			
	AD	5,900,755	05/04/99	Toeppen et al			
	AE	6,215,363	04/10/01	Conte et al			
	AF	6,295,327	09/25/01	Takla			
	AG	6,445,230	09/03/02	Rupp et al			
	AH	4,680,778	07/14/87	Krinock			
	AJ	5,943,378	08/24/99	Keba et al			
	AJ	6,188,737	02/13/01	Bruce et al			
	AK	5,914,592	06/22/99	Saito			
	AL	5,789,954	08/04/98	Toeppen et al			
PC	AM	4,694,244	08/15/87	Whiteside et al			
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PC	AN	JP4105070	04/07/92	Japan			Abstract
	AO	JP5196641	08/06/93	Japan			Abstract
	AP	JP5264595	10/12/93	Japan			Abstract
	AQ	JP8220144	06/22/99	Japan			Abstract
	AR	JP9005362	01/10/97	Japan			Abstract
	AS	JP10163859	06/19/98	Japan			Abstract
	AT	JP11098876	04/09/99	Japan			Abstract
	AU	JP62003544	01/09/87	Japan			Abstract
	AV	EP 0 631 143	12/28/94	Europe			
PC	AW	EP 0 241 142	10/14/87	Europe			
OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
PC	AY		Roland E. Best, <i>The Software PLL, Phase Locked Loops</i> , 3 rd Edition, McGraw-Hill, New York, 1997, pp 229-249				
	AZ		<i>Using FPGAs for Digital Applications</i> , Actel Corporation, April 1996				
	BA		HP E4543A Q Factor and Eye Contours Application Software, Hewlett Packard, 1999				
	BB		Infinium DCA, Agilent Technologies, March 7, 2002				
PC	BC		Communication waveform measurements, Hewlett Packard, June 26, 1996				
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			APPLICANT Martin MILLER et al.			
			FILING DATE September 29, 2003		GROUP 2133	
U.S. PATENT DOCUMENTS						
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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
	BG					YES NO
	BH					Abstract
	BI					Abstract
OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
PC	BJ		Advanced Analysis of High-Speed Digital Communication Waveforms, Hewlett Packard, June 27, 1994			
PC	BK		R.E. Anderson and E. M. Foster, Design of an MPEG-2 Transport Demultiplexor Core, IBM, 1999			
PC	BL		Technology Standards, Tektronix Website (www.tek.com/Measurement/Solutions/tech_standards/index.html?wt=257)			
PC	BM		Communications Signal Analyzer, Tektronix Website (www.tektronix.com/optical)			
PC	BN		RT-Eye™ Serial Data Compliance and Analysis Software, Tektronix Website (www.Tektronix.com/accessories)			
PC	BO		Design of FIR Filters by Windowing, MIT Website, (http://web.mit.edu/6.555/www/fir.html)			
PC	BP		A New Digital PLL at the Technische Universitaet Berlin, Technische Universitaet Berlin Website (www.tdi.com/~gottsch/tuberlin.htm)			
PC	BQ		Low Jitter Digital PLL - ZL30407, Zarlink Semiconductor Website, (http://products.zarlink.com/product_portlets/new_timer.htm)			
PC	BR		Michael K. Williams, et al., A Discussion of Methods for Measuring Low-Amplitude Jitter, International Test Conference, Paper 28.1, pp 646-652			
PC	BS		Russ Brown, Quantam Corporation, "Eye Diagram Data", SCSI Physical Working Group, February 9, 2000			
PC	BT		Dave Fink, Tektronix "Introduction to Measurement Techniques and Analysis of Emerging Serial Data Standards", November 2002			
PC	BU		"Methodologies for Jitter Specification Technical Report" Rev 10, June 9, 1999			
PC	BV		Andy Baldman, University of New Hampshire "Description of XAUI Physical Layer Measurements Performed At The UNH Interoperability Lab", October 30, 2002			
PC	BW		University of New Hampshire Technical Document, "fast Ethernet" February 13, 2003			
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APPLICANT

Martin MILLER et al.

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AD	5,900,755	05/04/99	Toeppen et al			
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AF	6,295,327	09/25/01	Takla			
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AL	5,789,954	08/04/98	Toeppen et al			
AM	4,694,244	08/15/87	Whiteside et al			

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			APPLICANT Martin MILLER et al.				
			FILING DATE September 29, 2003		GROUP 2133		
			U.S. PATENT DOCUMENTS				
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BK		R.E. Anderson and E. M. Foster, Design of an MPEG-2 Transport Demultiplexor Core, IBM, 1999					
BL		Technology Standards, Tektronix Website (www.tek.com/Measurement/Solutions/tech_standards/index.html?wt=257)					
BM		Communications Signal Analyzer, Tektronix Website (www.tektronix.com/optical)					
BN		RT-Eye™ Serial Data Compliance and Analyzer Software, Tektronix Website (www.Tektronix.com/accessories)					
BO		Design of FIR Filters by Windowing, MIT Website, (http://web.mit.edu/6.555/www/fir.htm)					
BP		A New Digital PLL at the Technische Universität Berlin, Technische Universität Berlin Website (www.tdl.com/~gottsch/tuberlin.htm)					
BQ		Low Jitter Digital PLL - ZD30401, Zarlink Semiconductor Website, (http://products.zarlink.com/product_portlets/new_timer.htm)					
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	APPLICANT Martin Thomas MILLER et al.	
	FILING DATE September 29, 2003	GROUP 2133

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PC	AA	6,112,160	08/29/00	Salant et al.			
PC	AB	4,876,655	10/24/89	Carlton et al.			
PC	AC	5,180,971	01/19/93	Montijo			
PC	AD	6,522,122	02/18/03	Watanabe et al.			
PC	AE	5,432,791	07/11/95	Gancarcik			
PC	AF	6,539,318	03/25/03	Miller et al.			
PC	AG	6,356,127	03/12/02	Klipper et al.			
PC	AH	4,758,963	07/19/88	Gordon et al.			
PC	AI	4,843,309	06/27/89	Kareem et al.			
PC	AJ	6,571,186	05/27/03	Ward			
PC	AK	2003/0163266	08/28/03	Ward et al.			

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PC	AL	EP 0 444 875	09/04/91	Europe				
PC	AM	EP 1 244 241	09/25/02	Europe				
PC	AN	EP 1 074 845	02/07/01	Europe				
PC	AO	EP 1 118 866	07/25/01	Europe				
PC	AP	WO 00/60806	10/02/00	WIPO				

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PC	AQ	Dennis Dickerson, "Fiber Optic Test and Measurement (Chapter 8); Prentice Hall PTR, 1998, pps. 284-338
PC	AR	Adam Healey et al., "Fast Ethernet Consortium - 100 Base-TX PMD Test Suite", Version 2.4 and Version 2.5; InterOperability Lab, 1998-1999
PC	AS	Adam Healey, "Fast Ethernet Consortium Notebook", 1996-1997 14 pps.
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	AU	
	AV	

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/Phung Chung/	06/27/2006

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PC	AA	6,549,859	04/15/03	Ward			
PC	AB	5,714,878	02/03/98	Saito et al.			
PC	AC	2003/0004664	01/02/03	Ward et al.			
PC	AD	6,009,132	12/28/99	Sholtz			
PC	AE	5,978,742	11/02/99	Pirkerd			
PC	AF	5,761,434	06/02/98	Hewitt			
PC	AG	5,953,071	09/14/99	Van Zon			
PC	AH	6,615,148	09/02/03	Pickerd			
PC	AI	6,642,926	11/04/03	Letts			
PC	AJ	6,044,123	03/28/00	Takla			
PC	AK	5,999,163	12/07/99	Ivers et al.			
PC	AL	5,214,784	05/25/93	Ward et al.			
PC	AM	5,761,537	06/02/98	Sturges et al.			
PC	AN	6,311,138	10/30/01	Miller			
PC	AO	5,402,443	03/28/95	Wong			
PC	AP	6,643,346	11/04/03	Pedrotti et al.			

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Sheet 1 of 1

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PC	AA	6,546,345	04/08/03	Ghiasi			
PC	AB	6,278,357	08/21/01	Croushore et al.			
PC	AC	6,366,631	04/02/02	Nakayama et al.			
PC	AD	5,966,684	10/12/99	Richardson et al.			
PC	AE	5,631,759	05/20/97	Bogdan et al.	↓	↓	
AF							
AG							
AH							
AJ							
AJ							
AK							

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